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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/806,003	06/15/2001	Maik Brett	55709	1311

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BOSTON, MA 02205

EXAMINER

NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
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2614

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/806,003

Applicant(s)

BRETT ET AL.

Examiner

Paulos M. Natnael

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The rejection under 35 USC 103 has been withdrawn and instead a rejection under **35 USC § 102** has been made. For that reason, this Office Action is made non-final.
2. The Examiner inadvertently wrote that Claims 14-28 were rejected, instead of Claims 14-26. The examiner regrets any confusion and/or inconvenience that may have caused the Applicant.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **14-26** are rejected under 35 U.S.C. 102(b) as being anticipated by **Braun**, U.S. Pat. No. 5,369,442.

Considering claim **14**, Braun meets all claimed subject matter, note;

a) wherein a sequence of insertion pictures ($K_j=K_1, K_2, \dots$) decimated by vertical decimation ($VD \geq 1$) are read into a memory device (S) and subsequently read out, wherein the insertion pictures (K_j) read out are inserted into a sequence of main pictures ($H_i=H_1, H_2, \dots$), is met by the insertion pictures K_1 and K_2

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inserted by the inserting device ES into a sequence of main signals H1 and H2,

Fig. 2;

b) wherein the memory device (S) has a storage capacity of less than two insertion pictures (K_j) and is subdivided into memory segments (X,Y,Z;A,B,C,D,E) which are continuously overwritten by the insertion pictures, is met by the disclosure (on col. 6, lines 46-51), "a memory device SP having two memory regions SP1, SP2 is also provided. The successive half-frames K.sub.1, K.sub.2 of the small picture K can be written or inscribed into these memory regions by means of a write-in or inscription device EN.

c) wherein a decision is made as to whether the currently written insertion picture (K_j) or the immediately preceding insertion picture (K_{j-1}) is read out, is met by the decision device EE outputting decision signal ROF, fig.2; (see col. 6, lines 60-65)

d) wherein more than one memory segment (X,Y,Z;A,B,C,D,E) of the memory device (S) is required for storing an insertion picture (K_j), and in that the memory segments (X,Y,Z;A,B,C,D,E) of the memory device (S) are cyclically overwritten by the insertion pictures (K_j) in a predetermined order, is met by SP1 and SP2 of memory SP, fig.2;

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Considering claim 15, the method of claim 14 wherein the memory segments (X,Y,Z;A,B,C,D,E) are the same size, is met by SP1 and SP2 of memory SP, fig.2;

Considering claim 16, the method of claim 14 wherein in a manner dependent on the ratio of a reading speed of a read pointer to a writing speed of a write pointer and a relative position of the write pointer in a writing area (I,II; I,II,III) holding the currently written insertion picture, a decision is made as to whether the currently written insertion picture (Kj) or the immediately preceding insertion picture (Kj-1) is read out.

See rejection of claim 1(c).

Considering claim 17, the method of claim 14 wherein the memory device has a storage capacity which is $(2^{-1}/VD)$ times the storage capacity required for an insertion picture, where VD is the vertical decimation of the insertion picture, is met by the disclosure that "the capacity of the memory device can, for instance, be selected in such a way that 288 lines times 270 picture elements (pixels) can be stored, and thus one entire half-frame of the main picture. According to the invention, the first memory region SP1 is located in a memory portion SPL of a memory device SPO that is intended for the left half of the picture, and the second memory region SP2 is located in a memory portion SPR provided for the right half of the picture." (col. 12, 35-39)

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Considering claim 18, the method of claim 17 wherein the memory segments are the same size and the number of memory segments is $2 \times VD - 1$, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).

See rejection of claims 17 and 15;

Considering claim 19, the method of claim 18 wherein a memory segment has a storage capacity of $1/VD$ times the storage capacity required for an insertion picture and the decision criterion that is applied is whether the last memory segment (II; 111) required for the currently written insertion picture is already being written too, is met by the SP1 and SP2 of memory SP, fig.2; (see also rejection of claim 17)

Considering claim 20, the method of claim 14 wherein the insertion pictures (K_j) and main pictures (H_i) are fields of a monitor picture, is met by the insertion pictures $K1/K2$ and main pictures $H1$ and $H2$, fig. 2;

Considering claim 21, the method of claim 14 wherein a comparison is made to determine whether a main picture (H_i) and an insertion picture (K_i) to be inserted into the latter have an identical field position, and, in the case of a differing field position, an identical field position is achieved by address shifting of the main picture (H_i) or of the insertion picture, is met by the disclosure that "The thus-obtained signal OFF is used as a decision criterion for the readout from the first

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or second memory region SP1, SP2. This is accomplished by sampling the signal OFF with the signal LZ 27, which defines the beginning of a half-frame in the main picture." (col. 10, 59-64)

Considering claim **22**, a circuit arrangement for picture-in-picture insertion having a memory device (S) for storing vertically decimated insertion pictures ($K_j = K_1, K_2$), the memory device (S) having a storage capacity of less than two insertion pictures (K_j) and being subdivided into memory segments (X,Y,Z;A,B,C,D,E) which can be continuously overwritten by the insertion pictures (K_j), having a control device (3) for reading out the vertically decimated insertion pictures from the memory device (S) and for inserting the insertion pictures (K_j) read out into a sequence of main pictures ($1 \leq i \leq H$ 1, H2...), and having a decision device for deciding whether the currently written insertion picture (K_j) or the immediately preceding insertion picture (K_{j-1}) is read out, wherein each memory segment (X,Y,Z;A,B,C,D,E) has a storage capacity of less than one insertion picture (K_j), and in that the memory segments (X,Y,Z;A,B,C,D,E) of the memory device (S) can be cyclically overwritten by the insertion pictures (K_j) in a predetermined order.

Regarding claim **22**, see rejection of claim **14**;

Considering claim **23**, the circuit arrangement of claim 22 wherein the memory segments (X,Y,Z;A,B,C,D,E) are the same size.

Regarding claim 23, see rejection of claim 15;

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Considering claim **24**, the circuit arrangement of claim 22 wherein the memory device has a storage capacity which is $(2-1/VD)$ times the storage capacity required for an insertion picture, where VD is the vertical decimation of the insertion picture.

Regarding claim 24, see rejection of claim 17.

Considering claim **25**, the circuit arrangement of claim 24 wherein the memory segments are the same size and the number of memory segments is $2^* VD-1$, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).

Regarding claim 25, see rejection of claim 18;

Considering claim **26**, the circuit arrangement of claim 22 wherein in a manner dependent on the ratio of a reading speed of a read pointer to a writing speed of a write pointer and a relative position of the write pointer in a writing area holding the currently written insertion picture, the decision device decides whether the currently written insertion picture (K_j) or the immediately preceding insertion picture (K_{j-1}) is read out.

Regarding claim 26, see rejection of claim 16.

Response to Arguments

5. Applicant's arguments filed 9/20/04 have been fully considered but they are not persuasive.

Applicant's Arguments

Braun does not teach or suggest a method or circuit arrangement for picture-in-picture insertion, including a memory device with a storage capacity of less than two insertion pictures, where more than one memory segment is required for storing an insertion picture. On page 3 of the Office Action of 05/18/2004, it was admitted that Braun does not disclose a memory device having a storage capacity of less than two insertion pictures. The Examiner then cited an excerpt of Braun stating that "the memory device can store more than two small pictures" (see column 12, lines 31-48). However, Braun still does not teach or suggest a memory device for storing less than two insertion pictures. Moreover, there is no teaching or suggestion that more than one memory segment is required for storing an insertion picture.

Examiner's Response

Braun anticipates the claims. Specifically, Braun teaches that two successive half-frames are stored in the storage SP. (see col. 6, lines 46-51) (There are successive, which means the former frames are overwritten by the succeeding ones, since the capacity of the storage is two half-frames). Two half-frames are equal to one full frame. The latter (one full frame) is less than two insertion pictures, unless of course Applicant is willing to further define in the claims what exactly is meant by less than two insertion pictures. A frame is a picture. Braun

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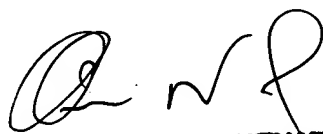
stores successive half-frames which are clearly less than two insertion pictures. Furthermore, Fig.1, small picture K clearly demonstrates the two half-frames of the picture. Therefore, the argument that Braun does not teach or suggest such a method is unpersuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



PAULOS M. NATNAEL
PATENT EXAMINER

PMN
January 10, 2005